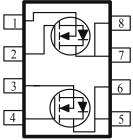
Dual N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low r_{DS(on)} Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)} m(\Omega) = I_D(A)$			
30	$34 @ V_{GS} = 10V$	6.9		
	$41 @ V_{GS} = 4.5V$	6.0		





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current ^a	T _A =25°C	I	± 6.9		
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	1 _D	± 5.6	А	
Pulsed Drain Current ^b		I _{DM}	± 40		
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	А	
Dower Dissinction ^a	T _A =25°C	P _D	2.1	W	
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	I D	1.3	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	t <= 10 sec	D	62.5	°C/W		
	Steady-State	R _{0JA}	110	°C/W		

Notes

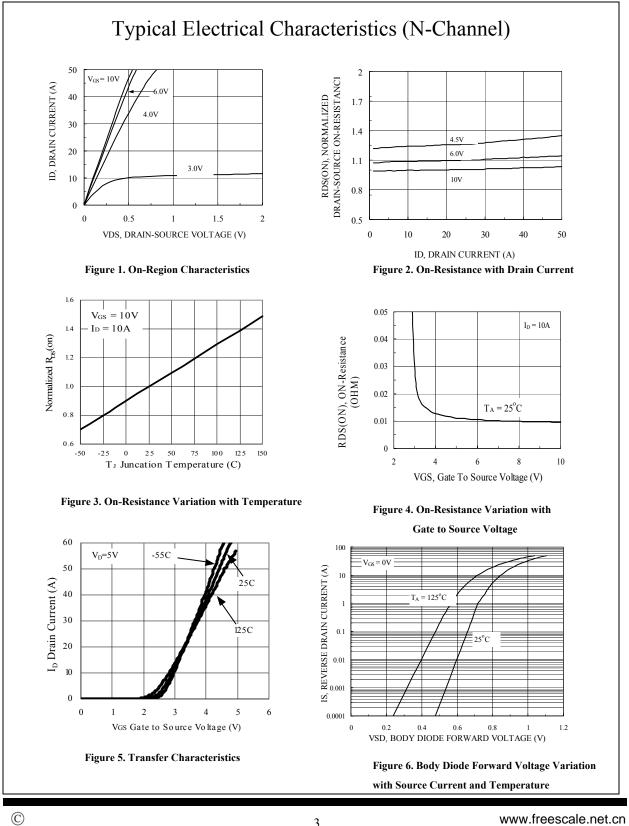
- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

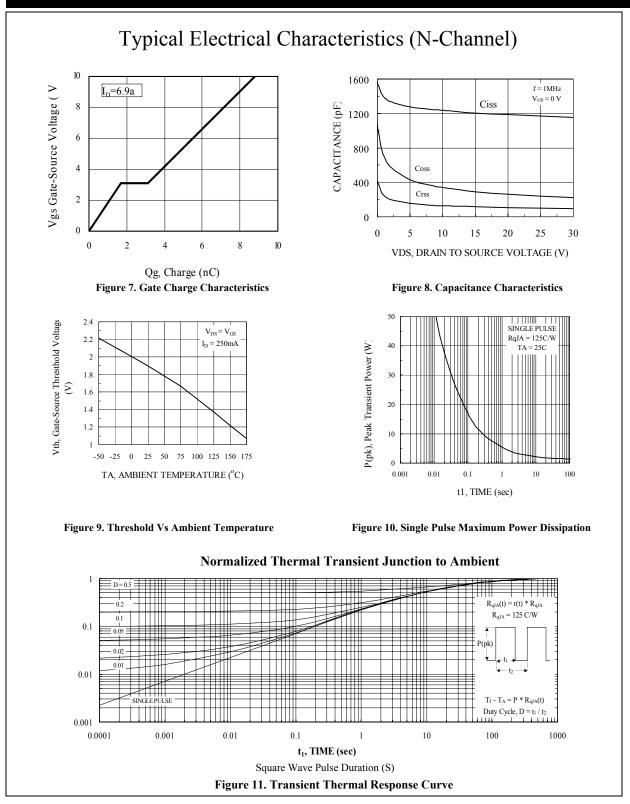
Parameter	S-makel Test Co.	Test Conditions	Limits			Unit
r al ameter	Symbol Test Conditions		Min	Тур	Max	Umt
Static						
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1			
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$			1	uA
Zero Gate Voltage Drain Current		$V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			10	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	20			Α
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 6.9 \text{ A}$			34	mΩ
Drain-Source On-Resistance		$V_{GS} = 4.5 \text{ V}, I_D = 6.0 \text{ A}$			41	
Forward Tranconductance ^A	g _{fs}	$V_{DS} = 15 \text{ V}, I_D = 6.9 \text{ A}$		25		S
Diode Forward Voltage	V _{SD}	$I_{\rm S} = 1.7$ A, $V_{\rm GS} = 0$ V		0.77		V
Dynamic ^b						
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 6.9 \text{ A}$		4.0		nC
Gate-Source Charge	Q _{gs}			1.1		
Gate-Drain Charge	Q _{gd}			1.4		
Turn-On Delay Time	t _{d(on)}			12		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, \text{ R}_{L} = 15 \Omega$, $\text{ID} = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}$ $I_{F} = 1.7 \text{ A}, \text{ Di/Dt} = 100 \text{ A/uS}$		10		nS
Turn-Off Delay Time	t _{d(off)}			60		
Fall-Time	t _f			15		
Source-Ddrain Reverse Recovery Time	t _{rr}			50		

Notes

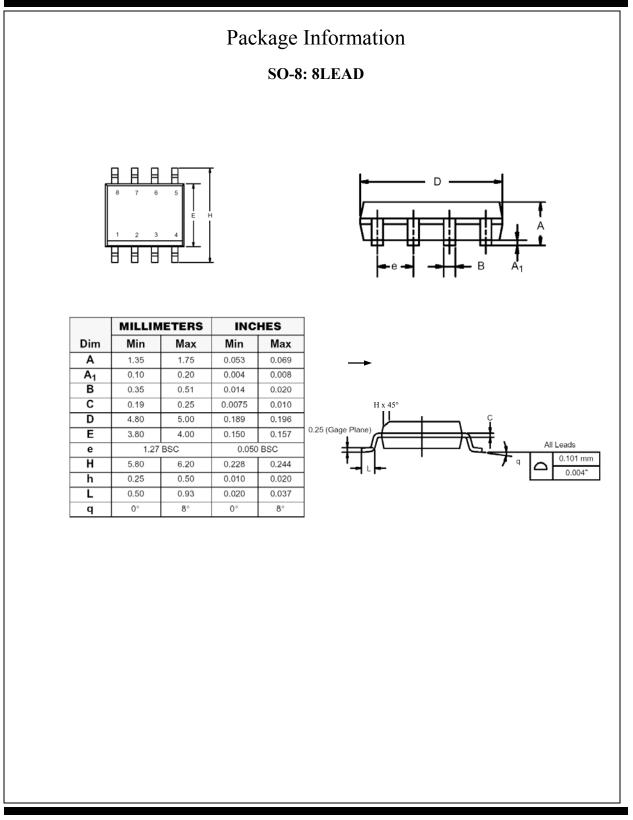
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Ordering information

- AM4920N-T1-XX
 - A: Analog Power
 - M: MOSFET
 - 4920: Part number
 - N: N-Channel
 - T1: Tape & reel
 - XX: Blank: StandardPF: Leadfree